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(54) MONOLITHIC SEMICONDUCTOR ARRANGEMENTS

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the manufacture of monolithic semiconductor arrangements.

According to the invention there is provided a method of making a monolithic semiconductor arrangement including the successive steps of forming an insulating layer on a body of semiconductor material of one conductivity type, forming a layer of silicon on the insulating layer, forming a layer of silicon nitride on the layer of silicon, etching away windows in the silicon nitride layer, etching away the silicon layer where it is exposed through the windows in the silicon nitride layer, introducing impurity through the windows in the silicon nitride and silicon layers into the semiconductor body to form regions therein of different conductivity to that of the body and removing the silicon nitride layer.

How the invention can be carried into effect will now be described by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figures 1 to 6 illustrate a monolithic semiconductor arrangement in successive stages of manufacture.

The fabrication of a monolithic semiconductor arrangement comprising a self-aligned FET and a charge-coupled device will be described.

A monocrystalline body 10 (Figures 1 to 6) of semiconductor material is preferably of P type silicon having a resistivity of about 10 ohm-centimeters. This resistivity indicates that the material of body 10 has an impurity concentration of about 10^{15} impurity atoms per cubic centimetre. To produce a charge-coupled array the resistivity of the starting material should be as high as possible. However, because an FET is to be formed in the same body 10 the resistivity must be lowered because of the requirements of the FET characteristics. Desirably for FET devices the resistivity should be 10 ohm-centimetres or less.

Although for the purposes of describing this embodiment, reference will be made to P type semiconductor material, it should be understood that material of the opposite conductivity type may also be used.

Following cleaning of the uppermost surface 11 of the body 10, a layer 12 of silicon dioxide 600 angstroms thick is formed thereon. This layer 12 can be produced by a thermal oxidation process by heating the semiconductor body to 1100°C and 1200°C, in a hydrogen atmosphere containing a small amount of oxygen for about twenty minutes.

Following the establishment of the silicon dioxide layer 12, a silicon nitride layer 13, having a thickness of 150 angstroms, is formed over layer 12. One particular method of forming such silicon nitride coatings, comprises a treatment in which silane and ammonia are mixed, in a carrier gas stream of hydrogen, and introduced into a chamber containing the silicon body at a temperature of about 900°C. At this temperature a reaction occurs, involving a decomposition of the silane, which results in the deposition of the silicon nitride layer 13 on the silicon dioxide layer 12. The layer 13 need not be thicker than 150 Å.

After the deposition of the silicon nitride layer 13, a polysilicon layer 14, about 2000 angstroms thick, containing approximately 10^{16} p type impurities per cubic centimetre,

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is grown on the surface of the layer 13. This polysilicon layer 14 is formed by placing the body 10 in a chamber heated to about 900°C in the presence of a decomposed silane gas contained in a hydrogen stream. If desired, the layer 14 can be grown in the presence of a suitable dopant gas or it can be subsequently doped. If subsequently doped, the underlying silicon nitride layer 13 will act as a diffusion mask preventing the dopant from penetrating into the oxide layer 12. Over the polysilicon layer 14 there is now deposited a second layer of silicon nitride 15. This nitride layer 15 is 600 angstroms thick and is grown using the technique described above. Over this second nitride layer 15, a 3000 angstrom thick layer of silicon dioxide 16 is formed to provide a base for the adhesion of any subsequent photoresist layers which do not adhere well to silicon nitride. Preferably, the latter layer of silicon dioxide is formed by pyrolytic deposition at about 800°C.

Once all these layers of various materials have been deposited in the required thicknesses on the surface of the semiconductor body 10, a photoresist mask 17 is provided over the entire surface and exposed to permit the opening of a window 18 in the layers 13 through 17 to define two distinct islands 19 and 20 in the layers 13 to 16 as shown in Figure 2. The initial oxide layer 12 is not etched. Under Island 19 a self-aligned FET device will be produced and under island 20 a charge-coupled device channel will be created.

These islands 19 and 20 are formed by removing, in the region of window 18, the layers 13 through 16 of the various materials. This is accomplished by using a different etchant for each of the different materials. For example, the outermost silicon dioxide layer 16 is removed by dipping the photoresist coated unit in a solution of a buffered hydrofluoric acid so as to remove the unmasked portion of layer 16 underlying the window 18. However, since the hydrofluoric acid solution does not substantially attack silicon nitride, layer 15 is unaffected, thus the etching treatment using the hydrofluoric solution terminates upon reaching layer 15. Layer 15 is, in turn, removed by using a hot phosphoric acid which attacks only that portion of layer 15 which has been exposed by removal of layer 16 under window 18. Simultaneously, this hot phosphoric solution will also attack and dissolve the photoresist layer 17. However, since the photoresist layer 17 is no longer required as an etchant mask, it does not matter whether layer 17 remains on the surface of the silicon oxide layer 16 or not. The silicon oxide layer 16 itself is now the primary barrier to the etching action of the phosphoric solution; that is, the hot phosphoric solution can attack silicon nitride only in the region exposed by the previously opened window 18 in the layer 16.

Layer 14 is removed by subjecting the body to a buffered hydrofluoric acid solution. Since the photoresist layer has now been removed by the hot phosphoric solution used to open the window in layer 15, the layer 16 is exposed to the solution used to etch layer 14 and is also etched. However, because layer 16 is made substantially thicker than any of the other layers, it is not etched away, but only reduced in thickness. Once the appropriate opening is etched in layer 14, the unit is again subjected to a hot phosphoric solution to etch the required opening in layer 13. In this manner, the window 18 is extended towards the surface 11 through layers 13 to 16.

At this time gallium, or other acceptor impurities, are diffused or ion-implanted into the semiconductor body through window 18 to form an isolation diffusion 23 in the body. This diffusion 23 ensures that surface inversion problems will be avoided and provides electrical isolation between the region 21 underlying island 19, in which the FET is to be formed, and region 22, underlying island 20, in which the charge-coupled channel is to be formed. This diffusion 23 can be made in the form of a ring surrounding the island 19 and a ring surrounding the island 20. Thus this diffusion can be a portion of a field region protecting both the FET and the charge-coupled array from unwanted surface states.

The gallium so diffused in the body is prevented from diffusing anywhere else in the semiconductor body 10 except under window 18 by the layers overlying the surface of the device. The initial layer 12 of silicon dioxide formed on the surface of the semiconductor body being relatively thin will not act as a bar to such gallium diffusion. Although it is preferred that layer 12 remain on the surface 11 and the gallium diffusion occur through it, it can be removed if such is desired. Under some circumstances, this entire isolation diffusion step may be eliminated.

After the creation of isolation diffusion 23, the coated body 10 is heated to about 1050°C and exposed to an oxidizing atmosphere of steam so that a thermal oxide plug 24, as shown in Figure 3, will grow in the previously etched window 18. This oxide plug 24 grows only in the exposed window 18 and does not grow elsewhere because of the barrier action of the layers coating the body 10. Preferably, this plug is made relatively thick: that is, about 8000 angstroms or more.

A second photoresist and etching operation is now performed in island 19 to etch the various layers 12 through 16 to define a source window 25 and a drain window 26

FIG 3

in order to create an FET by using a self-aligned gate process in which the polysilicon layer 14 acts as the gate conductor and exists on the device prior to the creation of the source and drain. The layers 12 through 16 are removed as described above. Source and drain N+ diffusions 27 and 28 are now formed by a standard diffusion technique followed by the usual drive-in diffusion step. For the described semiconductor body 10 arsenic is preferably used as the diffusant to create the source and drain regions 27 and 28. With arsenic the diffusion temperature is 900°C. If desired these source and drain regions 27 and 28 could be formed by ion implantation. Following the formation of the source and drain regions 27 and 28, the exposed surface of the semiconductor material over the now-defined source and drain regions 27 and 28 is reoxidized by the thermal oxidation step described above to form oxide plugs 29 and 30 in the windows 25 and 26 as shown in Figure 4. These source and drain plugs are formed at this time to ensure protection of the source and drain regions 27 and 28 during subsequent processing and formation of the charge-coupled channel under the island 20. When the regions 27 and 28 are diffused this step is used to "drive-in" the diffusion 27 and 28. When ion implanted this step also serves to anneal the implanted regions.

To form the charge-coupled channel the entire semiconductor body 10 is again masked with a photoresist and the island 20 is etched using the above described procedures into a line of separate smaller segments 31, 32, 33 and 34, separated by openings 35, 36 and 37 as shown in Figure 4. Once again, the initial layer 12 is not removed. After the layers 13 to 16 are etched off, gallium or another P type dopant is diffused or ion-implanted into the body 10 under the opening 35, 36 and 37 to produce P+ regions 38, 39 and 40. Preferably, with the described starting material these regions 38, 39 and 40 should be made to have a concentration of P type impurities of between 10^{17} and 10^{18} impurity atoms per cubic centimetre. The oxide layer 12 is so thin that it does not appreciably interfere with either the diffusion or ion-implantation of these impurities and the semiconductor material exposed to the dopant, i.e., regions 38, 39 and 40 will be doped to a concentration higher than the concentration in the remainder of the body. The portion of the body under the oxide plugs 24, 29 and 30 and under the remaining silicon nitride and polyisilcon layers is protected and no impurities are introduced therein.

Following this diffusion of gallium, the body is again subjected to the thermal oxidation process and plugs of silicon oxide 41, 42 and 43 each having a thickness of approximately 3000 angstroms are formed in the openings 35, 36 and 37.

Following the growth of these oxide plugs 41, 42 and 43, they are masked and the remaining portions of silicon dioxide layer 16 and silicon nitride layer 15 are removed as shown in Figure 5.

Following the removal of all the silicon dioxide layer 16 and the silicon nitride layer 15, a photoresist layer 44 approximately 12000 angstroms thick is placed over the surface of the wafer and windows opened in it over the oxide plugs 41, 42 and 43. Once these windows are opened in the photoresist layer 44, a film 48 of conductive material approximately 300 angstroms to 500 angstroms thick is deposited over the entire wafer surface as shown in Figure 5. Preferably, the deposition of this conductive film is performed by means of a room temperature sputtering operation. A typical procedure for producing such a film is as follows: The entire unit is placed in a conventional sputtering system either dc or RF and the surface of the unit is coated with a film of the selected conductive material. Because the sputtered material is directed towards the top surface of the entire device, little or no sputtered material will adhere to the sides of the windows opened in the photoresist layer 44. Thus only the surface of the photoresist layer and the top surfaces of the plugs will be coated.

Generally, any solid conductive material is suitable for use as the conductive film 48. Suitable materials are, for example, chromium or molybdenum. In any event the sputtered film should have a thickness between 300 and 500 angstroms to achieve conductivity in the thin film. Once an acceptable thickness of film 48 has been formed, the coated unit is removed from the sputtering chamber and the photoresist layer 44 is stripped from the surface. The removal of the photoresist will also remove the film 48 deposited over it. It will however not affect the film 48 deposited over the oxide plugs 41, 42 and 43.

The unit is again masked and as shown in Figure 6 contact holes to the source and drain are etched. Following the etching of the source and drain contact holes, a series of conductive electrode strips 50, 51, 52, 53, 54 and 55 are laid down over the unit. The electrodes 50, 51 and 52 contact the source, gate and drain respectively, of the FET created in island 19. Electrode 52 also serves to couple the FET to the charge-coupled array. Electrodes 53, 54 and 55, together with electrode 52, act as electrodes to the charge-channel array created under island 20. Each of the strips 53, 54 and 55 joins together a single strip of polycrystalline layer 14 and an adjacent single strip of the conductive film 48. Because the film 48 exists

is grown on the surface of the layer 13. Th polysilicon layer 14 is formed by placi the body 10 in a chamber heated to abo 900°C in the presence of a decompos silane gas contained in a hydrogen strea If desired, the layer 14 can be grown in t presence of a suitable dopant gas or it c be subsequently doped. If subsequent doped, the underlying silicon nitride layer will act as a diffusion mask preventing d dopant from penetrating into the oxide lay 12. Over the polysilicon layer 14 there new deposited a second layer of silicon nitri 15. This nitride layer 15 is 600 angstror thick and is grown using the technique de cribed above. Over this second nitride lay 15, a 3000 angstrom thick layer of silic dioxide 16 is formed to provide a base f the adhesion of any subsequent photoresi layers which do not adhere well to silic nitride. Preferably, the latter layer of silic dioxide is formed by pyrolytic deposition about 800°C.

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over the top of the oxide plugs 40, 41 and 42, the electrodes 53, 54 and 55 can be made very narrow and need only to make contact between the polycrystalline strip and the adjacent film. Preferably, the strips 53, 54 and 55 are formed of a conductive material different from that of the film 48. Such electrode strips may be deposited by placing the unit in a conventional evaporator and a coating of a conductive material, such as aluminium load down over the entire surface using normal evaporation techniques. The unit is then removed from the evaporator, masked and the excess aluminium etched away. In this etching step it is necessary that an etchant be used that will attack the exposed aluminium but not attack the other materials. Such an etchant can be, for example, a solution consisting of phosphoric acid, nitric acid and water. The unit as described and shown in Figure 6 thus depicts an FET and a charge-channel array interconnected one with another through the medium of electrode 52.

Under some conditions and especially when ion-implantation is used to create the described structure the silicon nitride layer 13 need not be used since this layer 13 is used only to ensure that the region underlying the gate of the FET is not adversely affected by unwanted impurity diffusing through the gate oxide. This elimination of layer 13 not only simplifies the process but also eliminates the sandwich structure in the gate region which is known in the prior art to cause threshold voltage stability problems. Thus this modified process maintains the advantages of the self-aligned gate process while avoiding its disadvantages. The device as described further eliminates surface inversion and eliminates the probability of electrical discontinuities in the charge-coupled array, while simultaneously improving the charge density that can be carried in the charge-coupled channel.

Although the described embodiment uses aluminium for the electrode strips and chromium as the film on the surface of the plugs, these materials could be interchanged or other suitable conductive materials used in their place.

There has been described a monolithic semiconductor arrangement comprising a self-aligned Field Effect Transistor and a Charge-Coupled Array having a good capacity for storing charges. The arrangement is formed by depositing both polysilicon and silicon nitride layers over a silicon dioxide layer on the surface of a silicon body and selectively etching these layers so that suitable dopants may be diffused or ion-implanted into selected areas of the underlying silicon body to form, in the same semiconductor body, a charge-coupled array having a self-aligned Field Effect Transistor associated therewith. This process not onl in which the under the oxid is low, but also Effect Transist and a charge-c capacity for st formed also spaced depletio electrical disco the depletion array are avoid

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9. A method of producing a monolithic emiconductor arrangement substantially as escribed with reference to and as illustrated the accompanying diagrammatic drawings.

10. A monolithic semiconductor arrangement produced by a method as claimed in any of the preceding claims.

F. JOHN HOBBS,
Chartered Patent Agent,
Agent for the Applicants.

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1421363 COMPLETE SPECIFICATION
1 SHEET

FIG.1

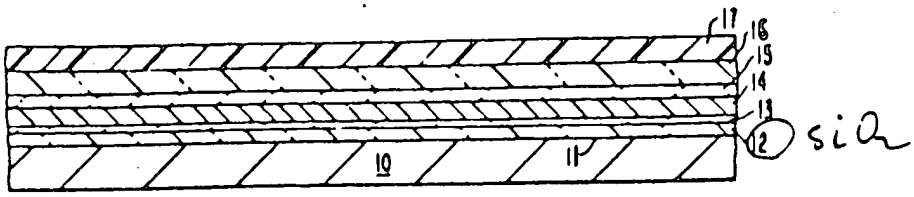

FIG.2

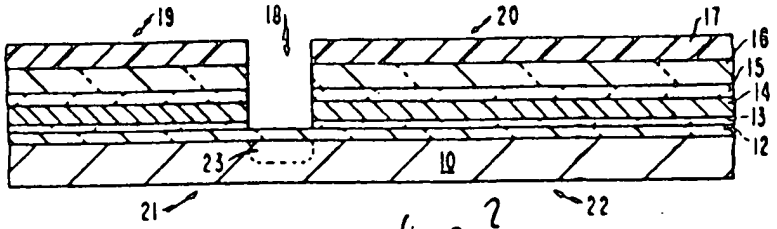

FIG.3

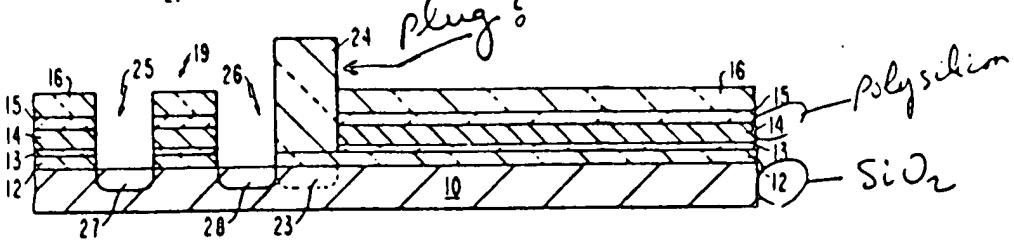

FIG.4

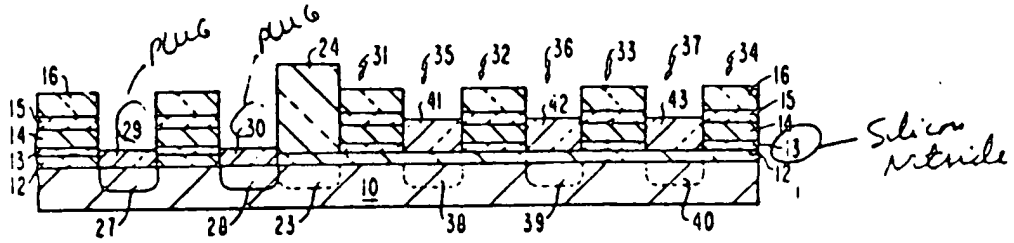

FIG.5

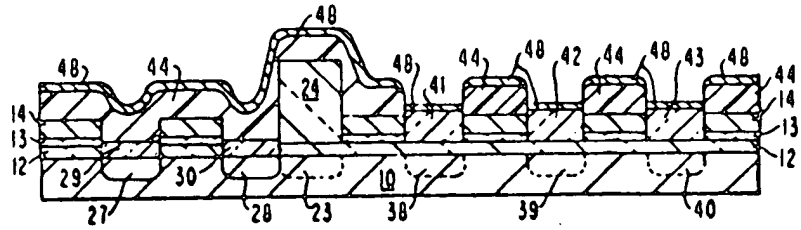

FIG.6